CAM:

- It is better to have a overall block diagram of the module.

Scan chain:

- If the image is too long, it is recommended to change the orientation rather than presenting it in two parts on the left and right sides.

- Synchronously reset the Flip-Flops when rst\_n == 1’b0.

- Please explain your design in more detail.

Built-in self test:

- Please explain your design with more detail.

FPGA:

-多加闡述你的設計

Take Away Part:

- Remember that all the DFFs have to be triggered by the system clock only.

- Yes, you can use a slower rate to take inputs from the button. There are some alternative design methods that you can consider. Howevver, the most important thing is to use only system clock to trigger the DFFs.

- If you have questions, we encourage to post on the discussion forum. I and the TAs will answer to those questions promptly.

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Simualtion results:

CAM: PASS

Scan chain: PASS

Built-in self test: PASS

Mealy machine sequence detector: FAIL